WHAT WE CLAIM ARE:

1. A semiconductor device, comprising a V-groove having V-shaped cross-section on a semiconductor substrate or on an epitaxial growth layer grown on a semiconductor substrate, and an active layer is provided only at the bottom of said V-groove.

2. A semiconductor device according to Claim 1, wherein said active layer is sandwiched between a cladding layer inside the V-groove and a cladding layer outside the V-groove, both cladding layers being in contact with each other on a side of said V-groove.

3. A semiconductor device according to Claims 1 or 2, wherein said active layer has a quantum well structure.

4. A semiconductor device according to Claim 2, wherein energy gap on the cladding layer outside the V-groove is greater than energy gap on the cladding layer inside the V-groove.

5. A semiconductor device according to Claim 1, wherein an inclined surface of said V-groove is a {111} B face.

6. A semiconductor device according to Claim 2, wherein an optical guiding layer having a refractive index lower than that of said active layer and higher than that of the cladding layer inside the V-groove is formed between said active layer and said cladding layer inside said V-groove.

7. A semiconductor device according to Claim 6, wherein conductivity type of the cladding layer inside said

V-groove is different from that of the cladding layer outside said V-groove.

8. A semiconductor device according to Claims 6 or 7, wherein conductivity type of the cladding layer inside said V-groove is identical with that of said optical guiding layer.

9. A semiconductor device according to Claims 6 to 8, wherein said active layer has a quantum well structure.

10. A semiconductor device according to Claim 6, wherein energy gap of the cladding layer outside said V-groove is greater than energy gap of the cladding layer inside said V-groove.

11. A semiconductor device according to claim 6, wherein an inclined surface of said V-groove is a {111} B face.

12. A semiconductor device according to Claim 6, wherein said V-groove is formed by vapor phase etching.

13. A semiconductor device according to Claim 2, wherein said active layer has distortion.

14. A semiconductor device according to Claim 13, wherein said active layer has a quantum well structure.

15. A semiconductor device according to Claim 13, wherein energy gap of the cladding layer outside said V-groove is greater than energy gap of the cladding layer inside said V-groove.

16. A semiconductor device according to Claim 13, wherein said V-groove is formed by vapor phase etching.

17. A semiconductor device according to Claim 13,

wherein said active layer has distortion.

18. A semiconductor device according to Claim 1, wherein said epitaxial growth layer is of double hetero structure with a first cladding layer and a seconed cladding layer having refractive index lower than that of a first optical guiding layer having higher refractive index, said active layer being in contact with said first optical guiding layer on a side of said V-groove, and a third cladding layer having refractive index lower than that of said active layer being provided on upper portion of said active layer inside said V-groove.

19. A semiconductor device according to Claim 18, wherein a second optical guiding layer having refractive index lower than that of said active layer and higher than that of said third cladding layer is provided between said active layer and said third cladding layer.

20. A semiconductor device according to Claims 18 to 20, wherein said first cladding layer and said first optical guiding layer are of the same first conductivity type, said third cladding layer and said second optical guiding layer are of the same second conductivity type, and said second cladding layer is of second conductivity type or has high resistance.

21. A semiconductor device according to Claim 18, wherein said V-groove is formed by vapor phase etching.

22. A method for manufacturing a semiconductor device, comprising the steps of forming a stripe-like etching protective film on a semiconductor substrate or on an

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